Amendments to the Specification:

Please make the following amendment to paragraph [41] of the application as filed, which is paragraph [87] of the application as published under Pub. No. 2004/0199674.

[41] The essential element of the interface circuit is an interface circuit chip 1, which has several I/O pins, which here are designated by pin A to pin D, and also a ground connection, which is designated by GND. These are the connections which realize the process connections; thus, e.g., data, measurement values, control commands, and the like are exchanged with external instruments or machines. The interface circuit chip 1, which is called simply chip 1 in the following, has two further connections IN, OUT for communicating with a logic circuit 3, which is formed, e.g., as an FPGA or ASIC. Here, the communication is realized over a **galvanic** decoupling device 2, which can be, e.g., an optocoupler, a magnetocoupler, a transformer, or some other known device for decoupling. The communication is realized bidirectionally, thus from chip 1 to logic circuit 3 via the connection OUT or vice versa from the logic circuit 3 to chip 1 via the connection IN.